



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,077	09/07/2003	Chien-Sheng Yang	ADTP0119USA	2076
27765	7590	07/31/2008		
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER CALEY, MICHAEL H	
			ART UNIT	PAPER NUMBER
			2871	
			NOTIFICATION DATE	DELIVERY MODE
			07/31/2008	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com  
Patent.admin.uspto.Rcv@naipo.com  
mis.ap.uspto@naipo.com.tw

<b>Office Action Summary</b>	<b>Application No.</b> 10/605,077	<b>Applicant(s)</b> YANG, CHIEN-SHENG	
	<b>Examiner</b> MICHAEL H. CALEY	<b>Art Unit</b> 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 July 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/7/08 has been entered.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al. (U.S. Patent No. 5,365,284 “Matsumoto”) in view of Kim (U.S. Patent No. 5,808,596) and Uehara et al. (U.S. Patent No. 6,329,980 “Uehara”).**

Regarding claims 1 and 2, Matsumoto discloses a method for manufacturing a thin film transistor liquid crystal display comprising:

- a panel (Figures 6A-6C);
  - a plurality of display cells (Figure 6C), each display cell having at least a thin film transistor (37);
  - a timing control circuit (120) for generating a timing signal (150); and
  - a plurality of logic circuits (50 and 60 or 30 and 55) for controlling operations of the display cells according to the timing signal;
- the method comprising:
- forming the plurality of display cells in the panel (Figures 6A-6C);
  - forming the plurality of logic circuits in the panel, wherein at least two logic circuits have the same function (Figure 6A).

Matsumoto fails to explicitly disclose determining a location in the panel for forming the timing control circuit so as to make differences among delay time intervals of the timing signals transmitted to different logic circuits less than 1000 microseconds, and forming the timing control circuit accordingly. Kim, however, teaches placement of the timing control circuit such that delivery of the timing signals to the different logic circuits having the same function is simultaneous (Figure 1; abstract; Column 3 lines 48-57).

Art Unit: 2871

It would have been obvious to one of ordinary skill in the art at the time the invention was made to transmit timing signals to different logic circuits with a difference of delay of less than 1000 microseconds. One would have been motivated to synchronize delivery of such signals to benefit from a high resolution without increasing clock frequency (abstract).

Matsumoto also fails to disclose the thin film transistor as a polysilicon thin film transistor. Uehara, however, teaches a polysilicon thin film transistor as advantageous to increase operating speed and aperture ratio and to decrease manufacturing cost (Column 1 lines 32-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the thin film transistor disclosed by Matsumoto as a polysilicon thin film transistor. One would have been motivated to form the transistor as a polysilicon thin film transistor to benefit from an increased operating speed and aperture ratio and to decrease manufacturing cost (Column 1 lines 32-48).

Regarding claims 3 and 4, Matsumoto discloses a plurality of scan lines (80) and data lines (70) connected to the display cells and a scan line driving circuit (50) connected to the plurality of scan lines and a data line driving circuit (30) connected to the plurality of data lines. Matsumoto fails to disclose first and second data line driving circuits in which data lines of the first and second driving circuits being arranged alternately. Kim, however, teaches such an alternate arrangement (Figure 1 elements 300, 310; abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form first and second data line driving circuits in which data lines of the first and second driving circuits are arranged alternately. One would have been motivated to form the driving circuits and data lines in such a manner to improve the resolution of the display.

Regarding claim 5, Matsumoto fails to disclose an interface circuit for receiving and transmitting an image signal such that the display cells operate according to the image signal. Kim, however, teaches such an interface circuit (Figure 1 element 500; abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an interface circuit as taught by Kim in the display disclosed by Uehara. One would have been motivated to add such an interface circuit as a means driving the second data line driver to improve the resolution of the display (Kim: abstract).

### ***Response to Arguments***

Applicant's arguments filed 7/7/08 have been fully considered but they are not persuasive.

Regarding claim 1, on Page 4 of Remarks, Applicant argues that the prior art fails to disclose or suggest the timing signals as transmitted to “different logic circuits with the same function”. Matsumoto, however, teaches different logic circuits with the same function (Figures 6A-6C [50 and 60] or [30 and 55]).

Regarding claims 2-5, Applicant further argues that the prior art fails to disclose or suggest a “relative physical location between the timing control circuit and the other logic

Art Unit: 2871

circuits in order to solve the delay time intervals..." (Page 5 Remarks) and that the prior art only accounts for an ideal timing delay (Pages 5-6). Kim, however, teaches placement of the timing control circuit and circuits having the same function "such that signals (b) and (c) are synchronized". Synchronization of signals must take into account every physical phenomenon such as relative physical location, differences between resistance values and capacitance values and their effect on delay, etc. Kim teaches a physical implementation of synchronized signals and therefore accounts for all reasons for delay differences between the transmitted timing signals.

### ***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL H. CALEY whose telephone number is (571)272-2286. The examiner can normally be reached on M-F 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2871

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael H. Caley/  
Primary Examiner, Art Unit 2871